AMENDMENTS

IN THE CLAIMS:

Please cancel claim 14 without prejudice or disclaimer, and please amend claims 11 and 19 as follows below:

1. (Withdrawn) A method of forming a semiconductor varactor, comprising:
forming a well region of a first conductivity type in a semiconductor substrate;
forming a gate dielectric layer on said well region;
forming a gate layer on said gate dielectric layer;
forming contact regions in said well region of a first conductivity type; and
forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie said well region.

2. (Withdrawn) The method of claim 1 further comprising forming sidewall structures adjacent to said gate layer.

3. (Withdrawn) The method of claim 2 wherein said well region is n-type.

4. (Withdrawn) The method of claim 2 wherein said well region is p-type.

5. (Withdrawn) The method of claim 1 wherein said forming gate layer contacts comprises forming said gate layer contacts to said gate layer over an active area of said semiconductor varactor.

6. (Withdrawn) A semiconductor varactor, comprising:
a well region of a first conductivity type in a semiconductor substrate;
a gate dielectric layer on said well region;
a gate layer on said gate dielectric layer;

contact regions in said well region of a first conductivity type; and

gate layer contacts to said gate layer wherein said gate contacts overlie said well region.

7. (Withdrawn) The semiconductor varactor of claim 6 further comprising sidewall structures adjacent to said gate layer.

8. (Withdrawn) The semiconductor varactor of claim 7 wherein said well region is n-type.

9. (Withdrawn) The semiconductor varactor of claim 7 wherein said well region is p-type.

10. (Withdrawn) The semiconductor varactor of claim 6 wherein said gate layer contacts comprises gate layer contacts to said gate layer over an active region of said semiconductor varactor.

11. (Currently amended) A method for forming a low resistance semiconductor varactor, comprising

providing a semiconductor substrate with at least a first isolation region and a second isolation region separated by a first distance;

forming a well region of a first conductivity type in said semiconductor substrate between said first isolation region and said second isolation region;

forming at least a first and second active regions in said well region by forming a contact isolation structure in said well region between said first isolation region and said second isolation region;

forming contact regions ~~on a~~ of the first conductivity type in said first and second active regions;

forming a gate dielectric layer on said first active region and said second active

region;

forming a gate layer on said gate dielectric layer wherein said gate layer overlies said first active region, said second active region, and said contact isolation ~~region~~ structure; and

forming electrical contacts to sad gate conductive layer wherein said electrical contacts are formed over said contact isolation ~~region~~ structure.

12. (Original) The method of claim 11 wherein said first and second isolation regions comprise STI structures.

13. (Original) The method of claim 11 wherein said contact isolation structure comprises a STI structure.

14. (Canceled).

15. (Withdrawn) A low resistance semiconductor varactor, comprising:

providing a semiconductor substrate with at least a first isolation region and a second isolation regions separated by a first distance;

a well region in said semiconductor substrate between said first isolation region and said second isolation region;

a contact isolation structure in said well region between said first isolation region and said second isolation region;

a gate dielectric layer on said well region and said contact isolation region;

a gate layer on said gate dielectric layer wherein said gate layer overlies said contact isolation region; and

electrical contacts to said gate conductive layer over said contact isolation region.

16. (Withdrawn) The varactor of claim 15 wherein said first and second isolation regions comprise STI structures.

17. (Withdrawn) The method of claim 15 wherein said contact isolation structure comprises a STI structure.

18. (Withdrawn) The method of claim 15 further comprising well contact regions adjacent to said first and second isolation regions.

19. (Currently amended) A method of forming a semiconductor varactor, comprising:

forming a well region of a first conductivity type in a semiconductor substrate;

forming a gate dielectric layer on said well region;

forming a gate layer on said gate dielectric layer;

forming contact regions of [[a]] the first conductivity type in said well region of a first conductivity type wherein said contact regions are formed using a source and drain region implantation formation process; and

forming gate layer contacts to said gate conductive layer wherein said gate layer contacts overlie an isolation region.

20. (Original) The method of claim 19 further comprising forming sidewall structures adjacent to said gate layer.

21. (Original) The method of claim 20 wherein said well region is n-type.

22. (Original) The method of claim 20 wherein said well region is p-type.